REMARKS

Claims 1-15 are pending. Claims 1-3, 9 and 10 were rejected under 35 USC 102(b) as being anticipated by Nakaya, US Patent No. 6,188,240. Claims 1, 14 and 15 were rejected under 35 USC 102(b) as being anticipated by New, US Patent No. 6,154,053. Claims 4-8 and 11-13 were indicated allowable if rewritten to overcome the rejections under 35 USC 112, second paragraph. The Advisory Action indicated that prior rejections under 35 USC 112 have been withdrawn.

35 USC 102(b): Claims 1 and 15

Independent claim 1 was rejected under 35 USC 102(b) as being anticipated by Nakaya. Claim 1 was also rejected under 35 USC 102(b) as being anticipated by New. Applicants respectfully disagree with both rejections, but have amended claim 1 to expedite prosecution. Claim 1 recites "an input line including a network of input lines and an input multiplexer... the input multiplexer is configured to receive input signals from at least one of the input lines and provide output signals to the K-LUT." Claim 1 also recites "an output line network including a network of output lines and an output multiplexer...the output multiplexer selects an output signal at outputs of the K-LUT" Support for the amendments can be found in several sections of the specification, including Figs. 3, 5, 7 and 9-12. As indicated in para. [0021] of the application, Fig. 3 illustrates a fracturable 6-LUT 300, which may be functionally understood as four 4-LUTs. Fig. 3, for example, includes 4-LUTs 302 and 304 and multiplexers 312 and 316. Multiplexer 312 receives input D and outputs to 4-LUT 302. Multiplexer 316 receives signals outputted by 4-LUTs 302 and 304.

On page 2 of the Office Action the examiner asserted that Figs. 17 and 34 of Nakaya disclose the features of claim 1. Fig. 34 illustrates a plurality of the structures shown in Fig. 17. Fig. 17 shows input blocks 3, logic blocks 2 and interconnection wires 8. The examiner equated the "K-LUT" of claim 1 with logic block 2 of Fig. 17. Fig. 17 depicts logic block 2 as having two outputs, C (carry out) and S (sum). Figs. 17 and 34, however, do not illustrate any multiplexers receiving the outputs C and S of logic block 2. Applicant's attorneys could not find any teaching or suggestion in Nakaya of multiplexers selecting among signals at the outputs of logic blocks or K-LUTs.

The invention of Nakaya, which relates to the use of improved function blocks within PLDs/FPGAs, would not easily accommodate the incorporation of output multiplexers in the manner of claim 1. (See col. 1, lines 4-7 and lines 30-33 of Nakaya.) Fig. 18 of Nakaya

indicates how the C (carry out) and S (sum) outputs of each programmable function block are received as inputs by other function blocks. Such interdependencies between function blocks are common in FPGAs. The introduction of an output multiplexer in each block, which may filter out output C or S, would seem to require a restructuring of the invention of Nakaya i.e. an alteration in the types and timing of signals that each function block expects from other function blocks. Such an alteration also seems to be a substantial departure from conventional FPGA architectures. Thus, Nakaya appears to teach away from the idea of including output multiplexers in the manner of claim 1.

On page 3 of the Office Action the examiner asserted that Figs. 6-12 of New also disclose the features of claim 1. Figs. 6-12 depict various carry logic circuits. (See col. 6, lines 47-49.) The carry logic circuits (e.g. circuits 100, 200, 300 and 400 in Fig. 6) add the input signals A_i, B_i and C_i to generate sum signals S_i. (See col. 8, line 26 of New). Figs. 6-12, however, do not teach or suggest including an input multiplexer that receives one of inputs A_i, B_i and C_i. Instead, the inputs A_i, B_i and C_i of Figs. 6-12 connect to exclusive OR gates (e.g. XOR gates 125-127 in Fig. 6), AND gates and/or OR gates.

Additionally, input multiplexers seem to conflict with the purpose of the invention in New. The invention of New relates to a carry logic circuit, which involves summing input signals. Input multiplexers may filter out some inputs in favor of others. A successful summing operation, however, requires using every one of the inputs to be summed. If one of A_i, B_i and C_i were removed by a multiplexer, the summing operation executed by, for example, circuit 100 of Fig. 6 would presumably fail. As a result, Fig. 6 and the invention of New appear to teach away from the inclusion of an input multiplexer.

Independent claim 15 was rejected under 35 USC 102(b) as being anticipated by New. Claim 15 has also been amended to recite "the input multiplexer is configured to receive input signals from at least one of the input lines." As explained above in connection with claim 1, New does not teach or suggest the inclusion of an input multiplexer in the manner of claims 1 and 15.

In view of the foregoing, it is respectfully submitted that claims 1 and 15 are patentable over the art of record. It is noted that the various independent claims differ from the cited prior art in a variety of other manners as well. However, since it is believed that the cited prior art clearly does not anticipate any of the pending claims for the reasons discussed above, the other distinctions are not articulated in detail in this response.

The various dependent claims are respectfully submitted to be patentable over the art of record for at least the same reasons as set forth above with respect to their associated independent claims. Furthermore, these dependent claims recite additional features that when considered in the context of the claimed invention, further patentably distinguish the art of record.

CONCLUSION

The Applicants believe that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution, Applicant's attorney, G. Audrey Kwan, can be reached at the telephone number set out below. If any additional fees are due in connection with the filing of this amendment, the Commissioner is authorized to charge such fees to Deposit Account 504480 (Order No. ALTRP196.)

Respectfully submitted,
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